DESCRIPTION
The DP-VPX-5843 is a VPX based Octal Digital Receiver Module, which measures the pulse parameters of Radar in the real time. This module is particularly suited for Radar systems where the signals are sampled at high rate with very high purity and to measure pulse parameters of Radar signals. For any DF (Direction Finding) systems, DP-VPX 5843 is optimized for gain and phase matching specifications.

BLOCK LEVEL EXPLANATION

Analog to Digital Converter (ADC)
The Ultra High Speed 1.5 GSOPS, Dual Channel, 10-Bit, Low Power ADC receives the IF input signals and digitize the analog inputs to digital using the 1350 MHz clock input. It achieves an excellent accuracy and dynamic performance while dissipating less than 3.63 Watts. The ADC has LVDS output interface for High Speed Data Transfer. The ADC has an improved internal track-and-hold amplifier and the extended self-calibration scheme to enable a very flat response of all dynamic parameters. This ADC achieves the SNR of 55dB and SFDR of 65dB.

FPGA
The board design incorporates two VIRTEX-7 485T series main FPGAs for processing the digitized data from the high speed ADCs and ARTIX-7 200T FPGA for user interface. The EEPROM and Flash PROM are interfaced with all the FPGAs. Each FPGA is interfaced with 8-bit DIP switches that enables external triggering to FPGA. The FPGAs are optimized for applications that require ultra-high Digital Signal Processing (DSP) performance and serial connectivity.

Memory
The board has 1 Gb Flash PROM. It offers a fast page access time of 25ns with a corresponding random access time as fast as 90ns. It features a Write Buffer that allows a maximum of 32 words / 64 bytes to be programmed in one operation, resulting in faster effective programming time than standard programming algorithms.

The board has three 2 Kb EEPROMs and three 256 Mb configuration PROMs interfaced with FPGAs.

KEY FEATURES AND BENEFITS
- Low power, 8 Channel, 10bit, 1.5GSOPS ADC LVDS outputs for ordering information DP-VPX-5843-600
- 8 Channel IF inputs
- IF Input signal upto +2dBm
- IF Frequency range from 50MHz to 1.4GHz
- High End Dual VIRTEX-7 485T and ARTIX-7 200T FPGAs
- High speed SERDES interface (sRIO, RIO, LVDS)
- Low speed data interface (LVTTL, TTL)
- 2 Kb EEPROMs, 256 Mb PROMs and 1 Gb interface with FPGA
- Temperature sensors
- High speed ADC mounting options available upto 8 channels, 12 bit, 2 GSOPS and 4 channels, 12 bit, 4 GSOPS

APPLICATIONS
- Radar signal digital down conversion
- IF signal processing
- Broadband data applications
- Communication systems
- Wideband EW system
JTAG Interface
The buffered daisy chained JTAG programming lines of all VIRTEX-7 and ARTIX-7 FPGAs are taken out through 14 pin JTAG header for In-System Programmable (ISP), also interfaced with P0 of VPX connector and through 9 pin micro D connector for integrated level programming.

VPX Interface
The DP-VPX-5843 has a standard VPX interface. The digitized output of the ARTIX-7 200T series FPGA is given through the VPX connector.

Clock Distribution
A 25MHz oscillator is used to provide a reference clock to the Frequency Synthesizer, which gives clock of 125 MHz to the FPGAs.

Transistor Transistor Logic (TTL) I/Os and Low Voltage TTL (LVTTL)
The FPGA has LVTTTL I/Os and TTL I/Os, from which 120 LVTTL I/Os and 48 TTL I/Os sent to the P4 and P5 VPX connector and the 51 pin micro D connector respectively. LVTTL I/Os is the level translator used to translate the LVCMOS I/Os into LVTTL I/Os. TTL I/Os is also a level translator used to translate the LVCMOS I/Os into TTL I/Os.

High Speed Interface (sRIO, RIO, LVDS)
The two VIRTEX-7 485T FPGAs are interfaced with 128 LVCMOS lines and 1 channel of x4 RIO lines for High Speed Inter FPGA data transfer. Each VIRTEX-7 485T FPGA is interfaced with ARTIX-7 200 T FPGA by 100 LVCMOS lines and 1 Channel of x2 RIO lines for High Speed Inter FPGA data transfer.

- The ARTIX-7 200T FPGA has two x 2 sRIO and two x4 sRIO channels on P1 of VPX connector
- The first VIRTEX-7 485T FPGA has two x4 RIO channels in P2 of VPX connector
- The second VIRTEX-7 485T FPGA has one x4 RIO channels and two x2 RIO channels in P2 of VPX connector
- Each VIRTEX-7 485T FPGA has 8 LVDS Transmitter lines and 8 LVDS receiver lines

Temperature Sensor
The temperature sensor monitors the temperature of all VIRTEX-7 and ARTIX-7 FPGAs, Four ADCs and bottom board temperature. The temperature sensor and over/under temperature alarm, with the added ability to automatically cancel the effect of resistance in series with the temperature monitoring diode.

Power Supply
The power supply is generated by dual channel buck converters and Low Drop Out (LDO) regulators. It monitors the generated voltages and distributes the supply voltages to the components in module.
## SPECIFICATIONS

### INPUT
- No. of IF channels: 8
- IF frequency range: 750 MHz to 1250 MHz
- IF signal range: Upto +2 dBm
- No. of sampling clock inputs: 4
- Sampling clock signal range: +3 to +10 dBm
- Gain matching: ±1.5 dB
- Phase matching: ±8º

### OUTPUT
- TTL: 48 bits, 1 channel of RS 232, 1 channel of RS 422 (Multiplexed with 4 lines of 48 TTL bits) on 51 pin Micro D connector
- JTAG signal on 9 Pin Micro D connector
- Two x 4 and two x 2 sRIO channels on P1 of VPX connector
- Three x 4 and two x 2 RIO channels on P2 of VPX connector
- 16 Transmitter lines of LVDS and 16 Receiver lines on P3 of VPX connector
- One channel of RS 422 signals and 60 Lines of LVTTL on P4 of VPX connector
- Three channels of RS 232 signals and 60 Lines of LVTTTL on P5 of VPX connector
- Two x 4 and two x 2 RIO channels on P6 of VPX connector

### MEMORY INTERFACE
- EEPROM: Upto 2 Kb
- Configuration PROM: Upto 256 Mb
- Data Flash: Upto 1 Gb

### POWER REQUIREMENTS
- Power supply: 12V ± 5%
- Power consumption: <70W

### MECHANICAL
- Dimension (in mm): 233.35(L) x 160(B) x 20(W)

### CONNECTORS
- RF Input: 8 SMP connectors for IF input signals and 4 SMP connector for clock signals on board (Front panel)
- Data connector: 51 Pin Sub-Miniature D connector and 9 pin Sub-Miniature D connector (Front panel)
- Standard VPX interface: VPX connector (P0 to P6)

### ENVIRONMENT
- Operating temperature: -40ºC to +70ºC
- Storage temperature: -40ºC to +70ºC
- Humidity: 95% RH
- Cooling: Conduction cooled

### ORDERING INFORMATION
- **ADC Mounting Options**
  - 00 - ADC-10D1500-ADCs for providing 8 Channel Outputs
  - 03 - ADC-12D1800-ADCs for providing 8 Channel Outputs
  - 06 - ADC-12D2000-ADCs for providing 8 Channel Outputs
  - 09 - ADC-16D3000-ADCs for providing 4 Channel Outputs
  - 30 - ADC-12D3600-ADCs for providing 4 Channel Outputs
  - 33 - ADC-12D4000-ADCs for providing 4 Channel Outputs
- 6 – Rugged Version