DATA PATTERNS

DP-cPCI-3996

64 Channel Digital Pattern Generator And Recorder Module

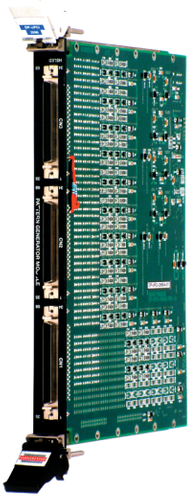
KEY FEATURES AND BENEFITS

- 64 channel digital pattern generation and recording
- 64x16K deep pattern memory independently available for generator, recorder, direction and control
- 15MHz pattern generation
- Segmentable pattern memory features
  - Start and Repeat pattern stores
  - Triggered start of pattern generation / recording / pre-post
  - Repeat pattern repeatable upto 64K times or continuously
- Arranged in 4 groups of 16 channels
- Pacer and trigger output of selectable polarity for external synchronisation
- Group wise features
  - Internal or external pacer
  - External pacer can be one of the selected groups
  - 32 bit counter for frequency control
  - Synchronisation between groups
  - Generation / Recording mode selected group
- 6U cPCI single slot
- Windows 2000 drivers provided
- RT Linux drivers provided

APPLICATIONS

- Pattern generator
- Pattern record & matching
- Digital bus signal test
- Semiconductor test
- Process control
- Automatic test equipment

DESCRIPTION



DP-cPCI-3996 is a 64-channel digital pattern generator and recorder. Each channel has 16Kbit deep pattern memory independently available for Pattern generator, recorder, direction and control. The Pattern memory may be used for both pattern generation and recording.

Pattern generation or recording may be achieved at a maximum clock speed of 15MHz.

The 64 Channels are grouped into 4 groups of 16 channels each. Each group may be individually configured as pattern generators or pattern recorders.

PATTERN GENERATION

The pattern to be generated is stored in pattern memory. Each channel has 16Kbit of pattern memory. A trigger initiates the Pattern generation and a pacer clocks the pattern generation. The location of the pattern memory that is utilized for pattern generation may be programmed. Pattern memory programming can include startup pattern memory and repeat pattern memory. Stages of pattern generation can generate triggers. Multiple groups may be simultaneously used for pattern generation. In this case, the groups may be synchronised together.

PATTERN GENERATION TRIGGERS

Pattern Generation may be triggered using any one or more of the following sources.

- External Trigger: A pulse signal from an external source may be used as a trigger.
- Other group trigger. End of pattern generation of startup pattern or repeat pattern generates trigger signals. These triggers can be used to trigger other groups.
- Software trigger: Trigger may be initiated by software command.

The Trigger signal is brought to the output connectors for external hardware synchronization. The polarity of the signal may be rising edge or falling edge under software control.

The valid triggers may be programmed or masked under software control.

PACER

The pacer controls the timing of the pattern generation. The pacer signal clocks the next pattern to be presented on the channel. The pacer signal may be from

- Internal clock
- External clock
- Pacer signal of any other group

The Pacer signal is brought to the output connectors for external hardware synchronization. The polarity of the signal may be active high or active low under software control.

PATTERN MEMORY UTILIZATION

Each channel has 16Kbit of pattern memory. Pattern memory may be flexibly programmed into multiple banks. The length of the bank may extend upto the entire 16Kbit of available memory.

The pattern may be programmed into two categories; the Startup Pattern and the Repeat Pattern. The startup pattern is generated upon trigger. The repeat pattern is generated repeatedly upto 64K times or continuously.

The repeat pattern is invoked as per user program:

- At the end of the startup pattern
- Repeat once on every trigger
- Never (repeat is not used).

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The location of the pattern within the pattern memory is programmed by setting the start address of the pattern. Startup pattern and Repeat pattern addresses are separately programmed. The number of times the “repeat pattern” is to be repeated is also programmable. These addresses are programmed groupwise.

SYNCHRONISATION

Pattern generation from multiple groups may be synchronised by the use of a common pacer for all the groups. Combining of pacer inputs between groups may be done under software control, without the need for external common wiring of pacer inputs.

PATTERN RECORDING

Digital Signals connected to the DP-cPCI-3996 may be recorded within the pattern memory of the Pattern Recorder. The signals may be clocked into the pattern memory from various clock sources. Pattern memory may be acquired on trigger. Data recorded in the pattern memory may be transferred to the cPCI bus. The amount of pre-trigger and post trigger data can be programmed.

PATTERN RECORDING CLOCK

The Pattern Recording is carried out on a synchronous basis with a clock source. The clock source is selectable on software control from:

- Internal Clock
- External Clock
- Clock signal of any other group

PATTERN RECORDING TRIGGERS

Pattern Recording may be triggered by any one or more of the following sources.

- External trigger: A pulse signal from an external source may be used as a trigger.
- Pattern trigger: Any pre-programmed bit pattern recognised in the group inputs can be used as a trigger
- Other group trigger. Trigger in any other group may be used as a trigger.
- Software trigger: Trigger may be initiated by software command.

The valid triggers may be programmed or masked under software control.

PRE TRIGGER AND POST TRIGGER

The number of samples prior to the trigger point that must be stored is programmable. The number of samples after the trigger point that must be stored is also programmable. The total of pre trigger samples and post trigger samples can extend until the full memory depth of 16K samples.

cPCI INTERFACE AND COMMON FACILITIES

The cPCI interface is a register based interface. The board is implemented as a 6U single slot module.

The Pattern memory is 64x16Kbit independently available for Pattern generator, recorder, direction and control. This is organized as 16 bit wide memory. The RAM cannot simultaneously read from the cPCI interface during pattern generation and recording.

The Pattern memory is shared between the Pattern Generation and Pattern Recording functions. Thus groups that are configured for recording cannot be used for generation and vice versa. Also, the contents of the Pattern RAM for a group must be reinitialised by software, whenever the group is changed to pattern generation mode.

SOFTWARE SUPPORT

The module is supplied complete with device drivers in Windows 2000 and RT Linux. Please contact factory for support in any other operating system such as VxWorks, QNX, INTime, Lynx etc.

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SPECIFICATIONS

No. of channel	64 channels programmable in 4 groups of 16 channels as pattern generation or pattern recording channels
Memory	64x16K bit independently available for pattern generator, recorder, direction and control
Channel type	TTL/CMOS compatible **
Maximum pattern rate	15MSa/sec

PATTERN GENERATION

Skew between channels	3ns typical
Rise time and fall time	7ns
Output high level	2.4V @16mA load
Output low level	0.4V @ 48mA load

PATTERN RECORDING

Input high levels	>2.0V
Input low levels	< 0.8V

EXTERNAL CLOCK

Maximum frequency	15MHz
Minimum pulse width	6ns

EXTERNAL TRIGGER

Minimum pulse width	6ns

TRIGGER SOURCES

Backplane trigger, external trigger, other group Trigger, software trigger, pattern trigger (Pattern recording mode only)

PACER CLOCK SOURCES

Internal clock, external clock, other group pacer

POWER

3.3V @ 2A

CONNECTORS

Backplane	cPCI
Field termination	3 x 68 pin SCSI connector

MECHANICAL

Board	233mm (H) x 160mm (D)

ENVIRONMENT

Commercial version only

ORDERING INFORMATION

DP cPCI 3996 3 0 0

- Factory options specified based on applications
- 3 - Commercial version

** Other options available

BLOCK DIAGRAM OF DP-cPCI-3996