DATA PATTERNS

DP-cPCI-3015

128 Channel Digital I/O With 6 Channel Counter

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KEY FEATURES AND BENEFITS

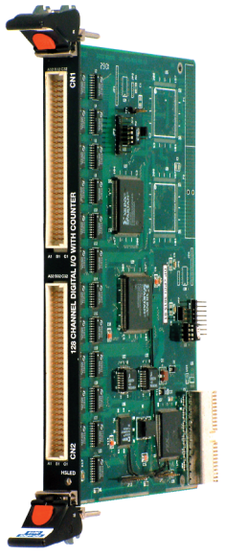
- 128 Channels of Digital I/O Programmable as Input or Output in groups of 16
- TTL/CMOS compatible Input / Output
- Input mode can be direct input, input interrupt, state change input or strobe input
- Two level latch output for simultaneous update of configured outputs
- 6 Channel 8254 compatible counter with all gate, source and output available for user control
- User programmable low true or high true logic for input
- Input and output can be used for self-test with field interface removed
- Debounce programmable for input in groups of 16
- Handshake for each group
- 6U cPCI single slot
- Hot swap compliant
- Windows 2000 drivers provided
- RT Linux drivers provided

APPLICATIONS

- High density DAQ system
- High density ATE
- Electronic & logic testing
- State change / interrupt monitoring
- Checkout systems
- TTL compatible outputs for soft PLCs

DESCRIPTION

DP-cPCI-3015 is a 128 channel TTL compatible Digital Input / Output card with 6 counter channels. The DIO can be programmed as input or output in groups of 16 channels.



INPUT

The inputs of the DP-cPCI-3015 is buffered with TTL compatible buffers. The inputs are processed through a debounce circuit to ensure that false transients are not recognised. The debounce time is programmable between 1μs to 16.77 seconds in 25 binary steps. Subsequent to de-bouncing the data can be acquired in a number of modes.

DIRECT INPUT

The debounced input data can be read on command from the host bus.

LOW TRUE & HIGH TRUE LOGIC

In case of inverted logic on the field signals, hardware corrections for the logic type can be achieved by activating the polarity control in the low true/high true logic selection block. The low true/high true polarity can be programmed on a per channel basis.

INTERRUPT MODE

Any input can be configured to generate an interrupt by programming the interrupt mask register. Whenever enabled input changes to its true state, an interrupt is generated.

STATE CHANGE INPUT

The state change input block continuously compares the current data with the previous data. Whenever the change occurs in the input the changed status is indicated via an interrupt and the changed channels are recorded for reading by the host through the cPCI interface.

HAND SHAKE INPUT

In hand shake input mode an input “strobe” signal latches the data on to the input latches. Simultaneously, interrupt is raised informing the host of availability of data. When the host reads the data, the ready for data signal is activated. One” strobe” signal and one “ready” for data signal is available for each group of 16 channels.

OUTPUT

Each of the 8 groups can be independently programmed as an output group. For output functions the data is written from the host onto a primary latch. Subsequently the host can give the command to latch this data onto the secondary latches. The secondary latch value is driven to the output lines with the TTL buffers. The latching to secondary latch can be carried out at the group level or for all 128 channels simultaneously.

OUTPUT HANDSHAKE

The data output process is provided with a hand shake capability. When the secondary latches have fresh data written on them a “data ready” signal is asserted. This indicates to the external hardware that it has data available to read. When the external hardware has read the data it can assert “request for data” signal. The request for data signal generates an interrupt to the host so that fresh data can be updated to the secondary latches.

SELF TEST REGISTER

A separate self-test register is available on the board. Data from the self-test register can be enabled via a multiplexer and read by the host to confirm read channel functionality. Output signals latched to the output buffers can also be read back for verification of the output signals. This readback can be carried out from the secondary latch stage. This readback is applicable for channels configured as outputs

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COUNTER

Six channels of 8254 compatible counter are available. Clock, gate and output signals are routed to the facia connectors. Gate is provided with a weak pull up and may or may not be connected externally. Counter output can be used to provide interrupt to the back plane thereby enabling use as a timer. Each channel can be programmed to any standard 8254 mode.

REAR I/O CAPABILITY

Additional 128 channels can be provided directly from optional FPGA to the J4, J5 rear I/O connectors. These are unbuffered channels.

cPCI INTERFACE

The cPCI interface is 32-bit 33 Mhz. The module is hot swap compliant as per PICMG2.1 Rev 1.0

SOFTWARE SUPPORT

The module is supplied complete with device drivers in Windows 2000 and RT Linux. Please contact factory for support in any other operating system such as VxWorks, QNX, INTime, Lynx etc.

SPECIFICATIONS

No. of Channels	128 configurable as Input or Output in groups of 16
Input Level	TTL/CMOS compatible V_{IH}>2V V_{IL}<0.8V
Output Level	TTL/CMOS compatible V_{OH}>2.4V@24mA V_{OL}<0.4V@48mA
Input	Modes: Direct Input, Strobe input, State change, Input/interrupt configurable per group basis Debouncing:Programmable from 1 sec to16sec Handshake: Data ready, acknowledge/group Interrupt: Interrupt is generated in any of the above mentioned mode Self Test: Output can be used to test input
Output	Modes: Two level latch Enable: Internal or External selectable Handshake: Strobe / group Self-Test: can read back the value through input without disturbing field wiring.
Counter	8254 compatible
Source	Internal clock or external clock programmed with gate can be external

POWER REQUIREMENTS	5V @ 1.5A, 3.3V @ 100mA
MECHANICAL Board	233 x 160mm
CONNECTOR	Module Single slot 6U(H), 4T (W) Backplane cPCI 6U Interface Field Interface 2 X 96 Pin Euro Front, Rear J4 & J5 connectors
ENVIRONMENT	Commercial and Rugged versions

ORDERING INFORMATION

DP cPCI 3015 3 0 0

- Factory options specified based on applications
- 0 - Front - 128 Channels
  3 - Rear - 128 Channels
  6 - Front & Rear - 256 Channels
- 3 - Commercial version
  6 - Rugged version

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BLOCK DIAGRAM OF DP-cPCI-3015