

DP-OBC-3006

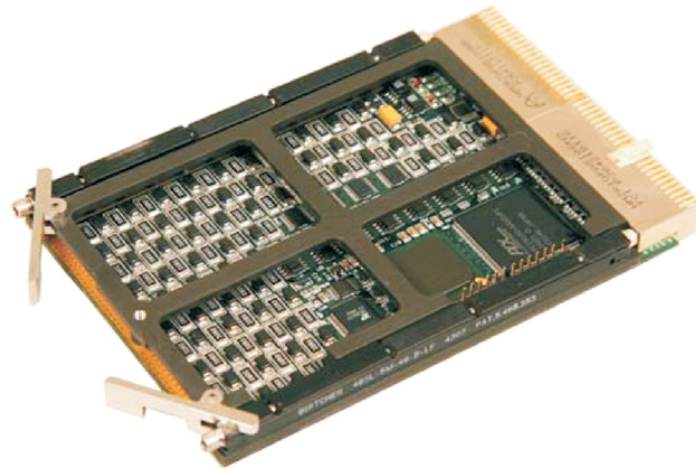
64 Channel Digital Output and 4 Channel RS422 Module

KEY FEATURES AND BENEFITS

- 64 channels of OPEN/GND outputs
- Darlington transistor array for high driving capacity
- 4 serial ports of RS-422, with isolated receivers
- 32 bit, 33MHz PCI bus interface
- FPGA for on-board logic
- VxWorks 6.3 drivers

APPLICATIONS

- Avionics
- Missile-borne application



DESCRIPTION

DP-OBC-3006 is a 3U cPCI-based board with 64 Digital Output channels and 4 ports of RS422 serial interface. It has 64 digital output channels in open/ground configuration and operates on 32-bit, 33MHz PCI bus. Four RS422 channels are incorporated with opto-isolated inputs which supports baud rates upto 115. Kbps.

DIGITAL OUTPUT INTERFACE

The open/ground output signals are generated by high-voltage, high-current Darlington transistor array which is driven by signals from FPGA. This array consists of seven NPN Darlington pairs which feature high voltage outputs with common cathode clamp diodes for switching inductive loads.

A series base resistor is provided for each Darlington pair, for operating directly with TTL or 5VCMOS devices. The collector current rating of a Darlington pair is 500mA. The output circuit is designed to accept a sink current of 150mA(max).

The output data is written from the host into a primary latch. Subsequently the host can give the command to latch the data onto secondary latches. The secondary latch value is driven to the output lines. The latching of data to secondary latch can be carried out for all 64 channels simultaneously. The built-in-self-test allows to test all the channels of the module independently without any external circuits.

The output is given as feed back for output failure detection such as fault detection of driver ICs. The feedback signals are given to the FPGA through 8 buffers (each having 8 channels). Each channel is pulled down in the board in order to maintain a default state during the configuration cycle of the FPGA. The output data is read back from two sources from the control logic, namely primary and secondary latches.

UART PORTS

An enhanced quad UART uses 128 bytes of transmit and receive FIFOs. It transmits and receives FIFO data, trigger levels, automatic hardware and software flow control signals. It supports data rates up to 115.2Kbps. Each UART has a set of register that provides user with operating status and control, receiver error indications and modem serial interface controls. Selectable interrupt polarity provides flexibility to meet design requirements. An internal loop back capability allows on-board diagnostics.

It provides parallel-to-serial (transmit) or serial-to-parallel (receive) data conversion over industry standard asynchronous data communication interface RS422 and logic levels TTL, CMOS etc.

SOFTWARE SUPPORT

The module is supplied complete with device drivers in VxWorks 6.3. Please contact factory for support in any other operating system such as Windows 2000, RTLinux, QNX, INTime, Lynx etc.

SPECIFICATIONS

OUTPUTS Digital Outputs 64 channels Open / Ground discrete output Output Current 150mA (max)		MECHANICAL Dimension in mm (LxBxW) 100±0.2 x 140±0.2 x 1.6±0.2 Module Standard 33MHz 32 bit 3U cPCI	
RS422 INTERFACE No of channels 4 Differential output voltage range 2V to 5V Common mode output voltage 2.5V (typ) Driver Current 25mA Baud Rate Up to 115.2 Kbps		CONNECTORS Backplane cPCI Interface Field Interface 100 pin I/O connector	
OPTO ISOLATED DIFFERENTIAL RECEIVER No of channels 4 Differential input voltage range 3.8V to 9V Input current 10mA (min-typ)		ENVIRONMENT Operating temperature -40°C to +70°C Storage temperature -40°C to +70°C Humidity 95% RH Cooling Conduction cooled	
POWER REQUIREMENTS Typical Power 2.6W Maximum Power 2.8W		ORDERING INFORMATION DP-OBC-3006-6XX 0 - Factory options specified based on applications 0 - 100±0.2 x 140±0.2 x 1.6±0.2 (LxBxW in mm) 3 - 100±0.2 x 160±0.2 x 1.6±0.2 (LxBxW in mm) 6 - Rugged Version	

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BLOCK DIAGRAM OF DP-OBC-3006

