DATA PATTERNS

# DP-OBC-3003

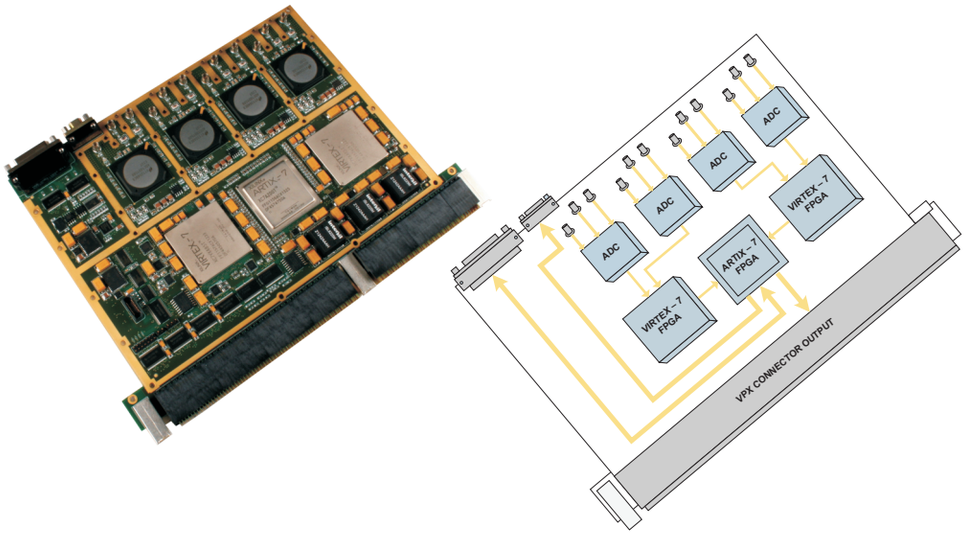
# 64 Channel Digital Input and 4 Channel RS422 Module

## KEY FEATURES AND BENEFITS

- 64 channels of OPEN/GND inputs
- 4 RS422 serial ports with isolated receivers
- 32 bit, 33MHz PCI bus interface
- On-board glue logic
- VxWorks 6.3 drivers

## APPLICATIONS

- Avionics and Missile-borne applications
- Military and space applications




## DESCRIPTION

DP-OBC-3003 is a rugged 3U cPCI based board with 64 Digital Input channels in open/ground configuration and 4 serial ports of RS422 interface. It operates on 32-bit, 33MHz PCI bus. Four RS422 channels are incorporated with opto-isolated inputs which supports baud rates upto 115.2Kbps.

## DIGITAL INPUT INTERFACE

The open/ground discrete input signals are converted to TTL signals by a level conversion circuit. These TTL signals are buffered and sent to the glue logic. Data is accessed from the glue logic through the PCI bus.

The following features are implemented in the digital input interface.

## SELF TEST

Complete built-in-self-test allows all channels in the module to be independently tested at glue logic register level, without any external circuit.

## INTERRUPT GENERATION

Input interrupt - Interrupts are generated when there is LOW to HIGH transition or HIGH to Low transition State change interrupt - Interrupts are generated if there is any change in the state of the inputs Software strobe interrupt - Interrupts are generated using software command Masking is done to disable the specified channel from generating an interrupt.

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## JTAG Interface

The buffered daisy chained JTAG programming lines of all VIRTEX-7 and ARTIX-7 FPGAs are taken out through 14 pin JTAG header for In-System Programmable (ISP), also interfaced with P0 of VPX connector and through 9 pin micro D connector for integrated level programming.

## VPX Interface

The DP-VPX-5843 has a standard VPX interface. The digitized output of the ARTIX-7 200T series FPGA is given through the VPX connector.

## Clock Distribution

A 25MHz oscillator is used to provide a reference clock to the Frequency Synthesizer, which gives clock of 125 MHz to the FPGAs.

## Transistor Transistor Logic (TTL) I/Os and Low Voltage TTL (LVTTL)

The FPGA has LVTTL I/Os and TTL I/Os, from which 120 LVTTL I/Os and 48 TTL I/Os sent to the P4 and P5 VPX connector and the 51 pin micro D connector respectively. LVTTL I/Os is the level translator used to translate the LVCMOS I/Os into LVTTL I/Os. TTL I/Os is also a level translator used to translate the LVCMOS I/Os into TTL I/Os.

## High Speed Interface (sRIO, RIO, LVDS)

The two VIRTEX-7 485T FPGAs are interfaced with 128 LVCMOS lines and 1 channel of x4 RIO lines for High Speed Inter FPGA data transfer. Each VIRTEX-7 485T FPGAs are interfaced with ARTIXS-7 200 T FPGA by 100 LVCMOS lines and 1 Channel of x2 RIO lines for High Speed Inter FPGA data transfer.

- The ARTIX-7 200T FPGA has two x 2 sRIO and two x4 sRIO channels on P1 of VPX connector
- The first VIRTEX-7 485T FPGA has two x4 RIO channels in P2 of VPX connector
- The second VIRTEX-7 485T FPGA has one x4 RIO channels and two x2 RIO channels in P2 of VPX connector
- Each VIRTEX-7 485T FPGA has 8 LVDS Transmitter lines and 8 LVDS receiver lines

## Temperature Sensor

The temperature sensor monitors the temperature of all VIRTEX-7 and ARTIX-7 FPGAs, Four ADCs and bottom board temperature. The temperature sensor and over/under temperature alarm, with the added ability to automatically cancel the effect of resistance in series with the temperature monitoring diode.

## Power Supply

The power supply is generated by dual channel buck converters and Low Drop Out (LDO) regulators. It monitors the generated voltages and distributes the supply voltages to the components in module.

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## SPECIFICATIONS

### INPUT

| | | |
|---|---|---|
| No. of IF channels | : | 8 |
| IF frequency range | : | 750 MHz to 1250 MHz<br>140 MHz to 180 MHz |
| IF signal range | : | Upto +2 dBm |
| No. of sampling clock inputs | : | 4 |
| Sampling clock signal range | : | +3 to +10 dBm |
| IF and sampling clock input impedance | : | 50Ω |
| Gain matching | : | ±1.5 dB |
| Phase matching | : | $8^{0}$ |

### OUTPUT

- TTL 48 bits, 1 channel of RS 232, 1 channel of RS 422 (Multiplexed with 4 lines of 48 TTL bits) on 51 pin Micro D connector
- JTAG signal on 9 Pin Micro D connector
- Two x 4 and two x 2 sRIO channels on P1 of VPX connector
- Three x 4 and two x 2 RIO channels on P2 of VPX connector
- 16 Transmitter lines of LVDS and 16 Receiver lines on P3 of VPX connector
- One channel of RS 422 signals and 60 Lines of LVTTL on P4 of VPX connector
- Three channels of RS 232 signals and 60 Lines of LVTTL on P5 of VPX connector
- Two x 4 and two x 2 RIO channels on P6 of VPX connector

### MEMORY INTERFACE

| | |
|---|---|
| EEPROM | Upto 2 Kb |
| Configuration PROM | Upto 256 Mb |
| Data Flash | Upto 1 Gb |

### POWER REQUIREMENTS

| | |
|---|---|
| Power supply | : 12V ± 5% |
| Power consumption | : <70W |

### MECHANICAL

| | |
|---|---|
| Dimension (in mm) | : 233.35(L) x 160(B) x 20(W) |

### CONNECTORS

| | |
|---|---|
| RF Input | : 8 SMP connectors for IF input signals and 4 SMP connector for clock signals on board (Front panel) |
| Data connector | : 51 Pin Sub-Miniature D connector and 9 pin Sub-Miniature D connector (Front panel) |
| Standard VPX interface | : VPX connector (P0 to P6) |

### ENVIRONMENT

| | |
|---|---|
| Operating temperature | : -40ºC to +70ºC |
| Storage temperature | : -40ºC to +70ºC |
| Humidity | : 95% RH |
| Cooling | : Conduction cooled |

### ORDERING INFORMATION

DP-VPX-5843-6XX

**ADC Mounting Options**

- 00 - ADC10D1500-ADCs for providing 8 Channel Outputs
- 03 - ADC12D1800-ADCs for providing 8 Channel Outputs
- 06 - ADC12D2000-ADCs for providing 8 Channel Outputs
- 09 - ADC10D3000-ADCs for providing 4 Channel Outputs
- 30 - ADC12D3600-ADCs for providing 4 Channel Outputs
- 33 - ADC12D4000-ADCs for providing 4 Channel Outputs

6 – Rugged Version

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## BLOCK DIAGRAM OF DP-OBC-3003